"VLSI DESIGN"

Good VLSI Design:➔ Besides realizing the desired specifications, a good VLSI Design must satisfy the following criterias or the following entities need to be optimized.

(i) Area ➔ Minimization of chip area is important to reduce the consumption of silicon wafer area and to increase the yield of the chip. [yield means, if you make 100 chips, how many are good out of 100, also , if the area of chip is small then yield is good.]

(ii) Speed ➔ The speed of a circuit needs to be increased. However increasing the speed increases the chip area. So the designer should consider the trade off between Area and Speed.

(iii) Power Dissipation➔ if a chip dissipates too much power it becomes too hot and cease working or needs extra/expensive cooling mechanism. Power Dissipation should be minimized for better performance. However reducing the power dissipation often necessitates the reduction of speed. So here exists a tradeoff between power dissipation and speed.

(iv) Design Time➔ the design time of an integrated circuit needs to be small, so that it is available at the market, at the earliest for economic reason.

(v) Testability➔ it is important that a chip is testable, because the test equipment and the testing process is often complex. Good testability requires more area. So here exists a tradeoff.

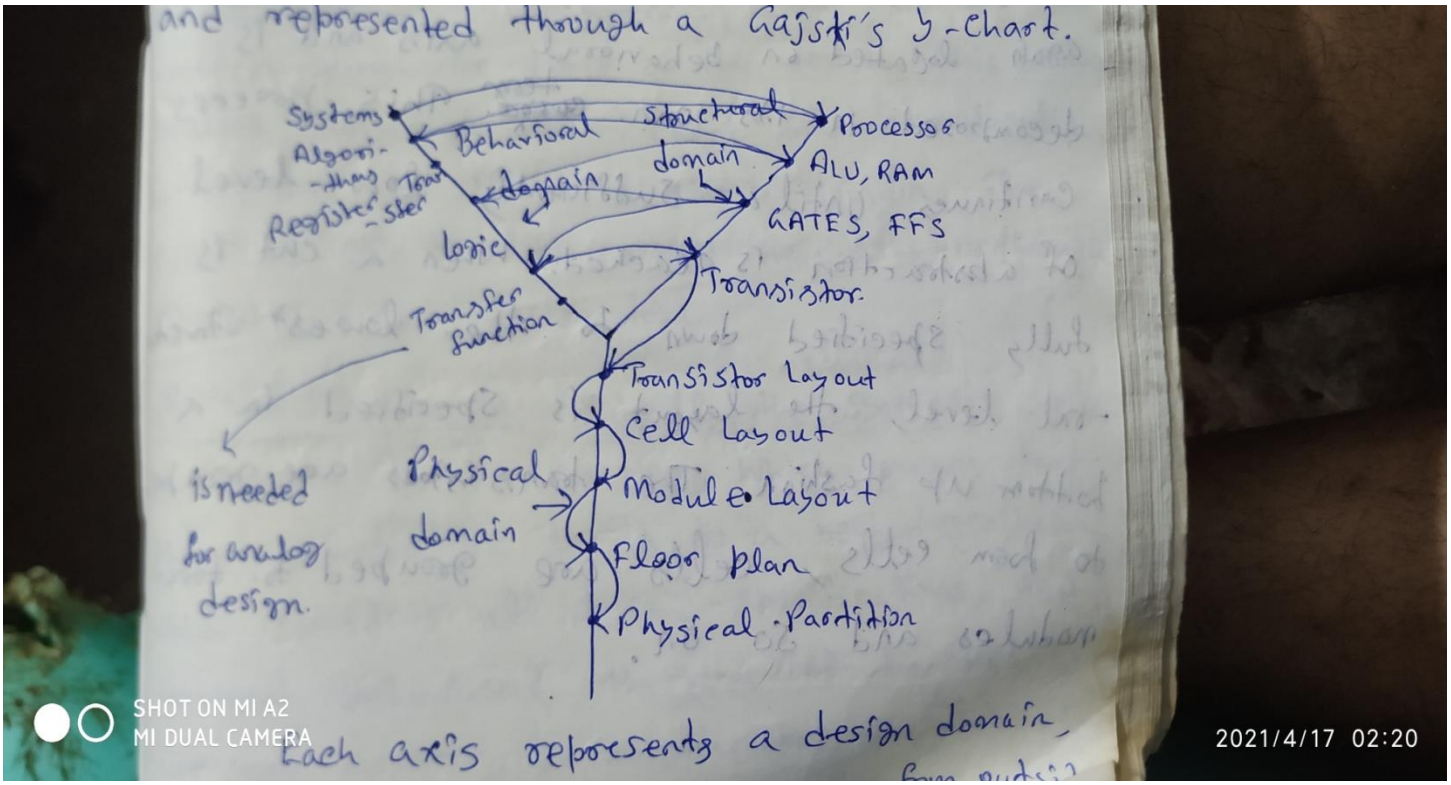
Deisgn Domain: Y chart➔ the VLSI design process is described in the following three domains.

(i) Behavioral Domain➔ in this domain, part of the design or the whole is seen as a black box. The relation between inputs and outputs are given without reference to the implementation of the relation.

(ii) Structural Domain➔ in this domain the circuit is described by a set of sub-circuits and the interconnection between them.

(iii) Physical Domain➔ the physical domain deals with actual geometry of the circuit, and describes the shape, size and locations of the components.

These three domains are interconnected and represented through Gajski's Y Chart.



Each axis represents a design domain and the level of abstraction decreases from outside to the centre.

Top Down Design Methodology➔ top-down design decomposition and bottom-up layout reconstruction. The above Y chart is a very powerful tool for describing the methodologies. The components with known behavior are decomposed into smaller blocks with simpler behavior and interconnection structure. This corresponds to transition from behavioral to structural domain. Each sub-component is again located on behavioral axis and is decomposed in its own term. This process continues until a sufficiently low level of abstraction is reached, when a circuit is fully specified down to the lowest structural level, the layout is specified in a bottom-up fashion. The transistors are grouped to form cells, cells are grouped to form modules and so on.