

**SURENDRANATH COLLEGE**

INTERNAL ASSESSMENT

SEMESTER-1, 2018-19

SUBJECT-Computer Science General (CMS-G)

CC-1-1-TH (Computer Fundamentals and Digital Logic Design)

Time- 01 Hr.

Full Marks-30

<b>CU Reg. No.-</b>	<b>SECTION-</b>	<b>ROLL NO.-</b>
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<b>MARKS OBTAINED</b>	Signature of Examiner- With date
<b>MARKS CONVERTED TO 10</b>	Approved by HOD- With date

*Your answer must fit within the provided space  
You may use the last page of your answer booklet for ROUGH work*

*Question Booklet < Total pages=12>*

*Answer question no. Q1 and any 4 from the rest (Q2 to Q9)*

**Q1. Answer any 4 questions out of 7 [Q1(a) to Q1(g)] .**

**4x1.5**

**(a) Write two important features of 3<sup>rd</sup> generation computer.**

**(b) Draw the truth table and logic diagram of a half adder.**

**(c) What is cache memory?**

**(d) Convert:  $(435.25)_{10} = (?)_2$**

**(e) Define seek time and latency time.**

***(f) Define combinational circuit and sequential circuits.***

***(g) Differentiate between static and dynamic RAM.***

**Q2. Answer any 4 questions out of 8 (Q2 to Q9)**

**Q2. (a) Compare between First and Second generation of computer. (b) What are impact printer and non impact printer? (4+2)**

**Q3. (a) Define System software and Application software with example. (b) Compare between Machine Language and Assembly language. (4+2)**

**Q4. Write short note on Any three of the following: (a) Memory Hierarchy (b) Von Neumann Architecture (c) CPU (d) Booting (e) BIOS (3X2)**

**Q5. (a) Find  $1001100 - (1100101$  using i. 1's complement method. ii. 2's complement method.  
(b) Find the dual of  $F = xy'z' + xyz'$  then draw the logic diagrams of its dual. (4+2)**

**Q6. (a) What are the universal gates? (b) Prove that NAND gate is a Universal Gate. (2+4)**



**Q7. (a) What is multiplexer? (b) Design a  $4 \times 1$  MUX and explain its working principle. (2+4)**

**Q8. (a) Draw the circuit Diagram of S-R flip-flop and state the truth table and excitation table of S-R flip-flop. (b) What is Race around condition? (4+2)**

**Q9. (a) Design a MOD 6 up counter using J-K flip-flop. (b) Differentiate between synchronous and asynchronous counter. (4+2)**

***Rough-work***